DATA SHEET

AAT1149: 3 MHz Fast Transient 400 mA Step-Down Converter

Applications

- Cellular phones
- Digital cameras
- Handheld instruments
- Microprocessor/DSP core/IO power
- PDAs and handheld computers
- USB devices

Features

- Ultra-small 0603 inductor (height = 1 mm)
- V_{IN} range: 2.7 V to 5.5 V
- V_{OUT} adjustable from 1.0 V to V_{IN}
- Max output current: 400 mA
- Up to 98% efficiency
- 45 μA no-load quiescent current
- 3.0 MHz switching frequency
- 70 μs soft start
- Fast load transient
- Over-temperature protection
- Current limit protection
- 100% duty cycle low-dropout operation
- Shutdown current: <1 μA
- Temperature range: –40 °C to +85 °C
- SC70JW (8-pin, 2.2 mm × 2 mm) package (MSL1, 260 °C per JEDEC-J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04-0074.

Description

The AAT1149 SwitchReg™ is a 3.0 MHz step-down converter with an input voltage range of 2.7 V to 5.5 V and output voltage as low as 1.0 V. It is optimized to react quickly to load variations and operate with a tiny 0603 inductor that is only 1 mm tall.

The AAT1149 output voltage is programmable using external feedback resistors. It can deliver 400 mA of load current while maintaining a low 45 μA no-load quiescent current. The 3.0 MHz switching frequency minimizes the size of external components while keeping switching losses low.

The AAT1149 maintains high efficiency throughout the operating range, which is critical for portable applications.

The AAT1149 is available in a Pb-free, space-saving 8-pin, 2.2 mm × 2.0 mm SC70JW package, and is rated over a –40 °C to +85 °C temperature range.

A typical application circuit is shown in Figure 1. The pin configuration is shown in Figure 2. Signal pin assignments and functional pin descriptions are provided in Table 1.

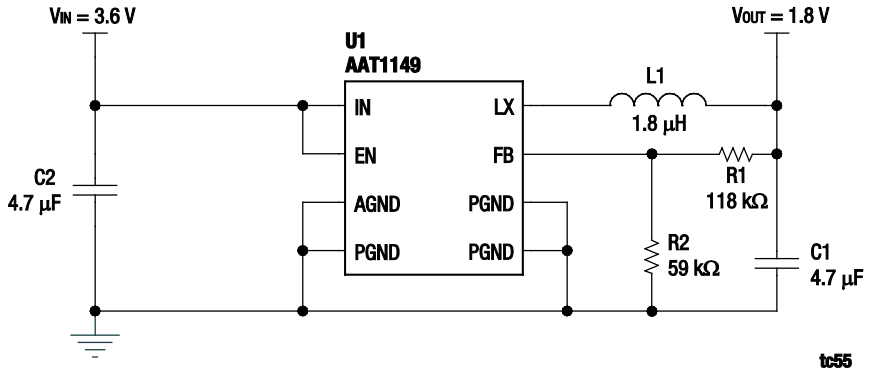


Figure 1. AAT1149 Typical Application Circuit

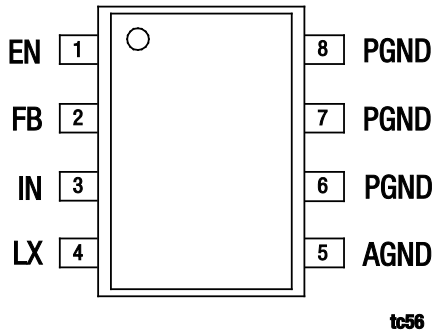


Figure 2. AAT1149 8-Pin SC70JW (Top View)

Table 1. AAT1149 Signal Descriptions

Pin #	Name	Description
1	EN	Enable pin.
2	FB	Feedback input pin. This pin is connected to an external resistive divider for an adjustable output.
3	IN	Input supply voltage for the converter.
4	LX	Switching node. Connect the inductor to this pin. It is internally connected to the drain of both high- and low-side MOSFETs.
5	AGND	Non-power signal ground pin.
6	PGND	Main power ground return pins. Connect to the output and input capacitor return.
7	PGND	Main power ground return pins. Connect to the output and input capacitor return.
8	PGND	Main power ground return pins. Connect to the output and input capacitor return.

Electrical and Mechanical Specifications

The absolute maximum ratings of the AAT1149 are provided in Table 2 and the electrical specifications are provided in Table 3.

Typical performance characteristics of the AAT1149 are illustrated in Figures 3 through 28.

Table 2. AAT1149 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Minimum	Typical	Maximum	Units
Input voltage to GND	V_{IN}		6.0		V
LX to GND	V_{LX}	–0.3		Vin + 0.3	V
FB to GND	V_{FB}	–0.3		Vin + 0.3	V
EN to GND	V_{EN}	–0.3		+6.0	V
Operating junction temperature	T_J	–40		+150	°C
Maximum soldering temperature (at leads, 10 seconds)	T_{LEAD}		300		°C
Maximum power dissipation (Note 2)	P_D		625		mW
Thermal resistance	θ_{JA}		160		°C/W

Note 1: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed may result in permanent damage to the device.

Note 2: Derate 6.25 mW/°C above 25 °C.

***CAUTION**: Although this device is designed to be as robust as possible, Electrostatic Discharge (ESD) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions should be used at all times.*

Table 3. AAT1149 Electrical Specifications (Note 1)
(V_{IN} = 3.6 V, T_A = –40 °C to 85 °C, Unless Otherwise Noted. Typical Values are at T_A = 25 °C)

Parameter	Symbol	Test Condition	Min	Typical	Max	Units
Step-Down Converter						
Input voltage	V_{IN}		2.7		5.5	V
UVLO threshold	V_{UVLO}	V_{IN} rising			2.7	V
		Hysteresis		100		mV
		V_{IN} falling	1.8			V
Output voltage tolerance	V_{OUT}	I_{OUT} = 0 to 400 mA, V_{IN} = 2.7 V to 5.5 V	–3.0		3.0	%
Adjustable output voltage range	V_{OUT}		1.0		V_{IN}	V
Quiescent current	I_Q	No load		45	70	µA
Shutdown current	I_{SHDN}	V_{EN} = GND			1.0	µA
P-channel current limit	I_{LIM}		600			mA
High side switch On resistance	$R_{DS(ON)H}$			0.45		Ω
Low side switch On resistance	$R_{DS(ON)L}$			0.40		Ω
LX leakage current	I_{LXLEAK}	V_{IN} = 5.5 V, V_{LX} = 0 to V_{IN}, V_{IN} = GND			1	µA
Line regulation	$\Delta V_{LINEREG}$	V_{IN} = 2.7 V to 5.5 V		0.1		%/V
Out threshold voltage accuracy	V_{OUT}	0.6 V output, no Load, T_A = 25 °C	591	600	609	mV
Out leakage current	I_{OUT}	0.6 V output			0.2	µA
Start-up time	t_S	From enable to output regulation		70		µs
Oscillator frequency	f_{OSC}	T_A = 25 °C		3.0		MHz
Over-temperature shutdown threshold	T_{SD}			140		°C
Over-temperature shutdown hysteresis	T_{HYS}			15		°C
EN						
Enable threshold low	$V_{EN(L)}$				0.6	V
Enable threshold high	$V_{EN(H)}$		1.4			V
Input low current	I_{EN}	V_{IN} = V_{OUT} = 5.5 V	–1.0		1.0	µA

Note 1: Performance is guaranteed only under the conditions listed in this Table.

Typical Performance Characteristics

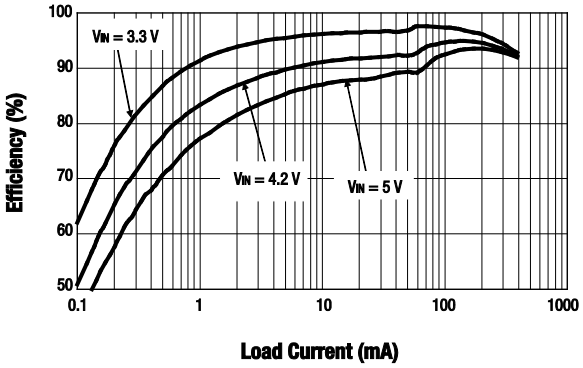


Figure 3. Efficiency vs Load Current (V_{OUT} = 3 V, L = 3 µH)

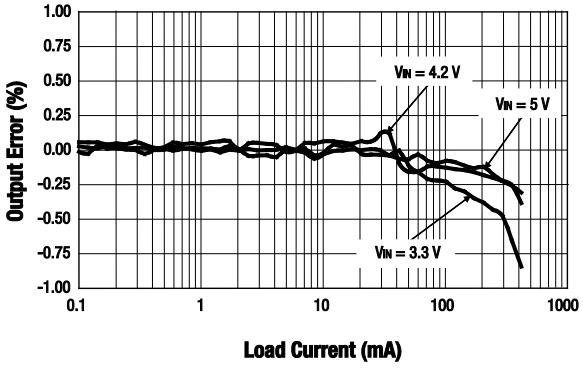


Figure 4. Load Regulation (V_{OUT} = 3 V, L = 3 µH)

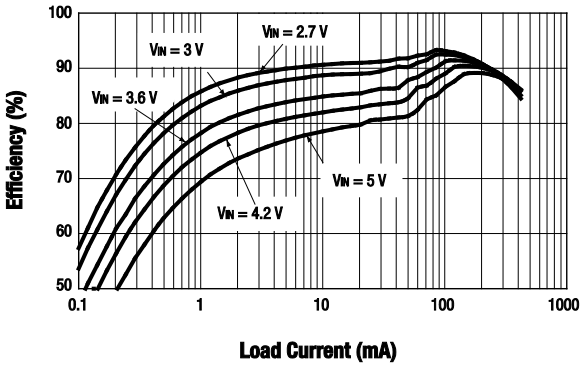


Figure 5. Efficiency vs Load Current (V_{OUT} = 1.8 V, L = 2.2 µH)

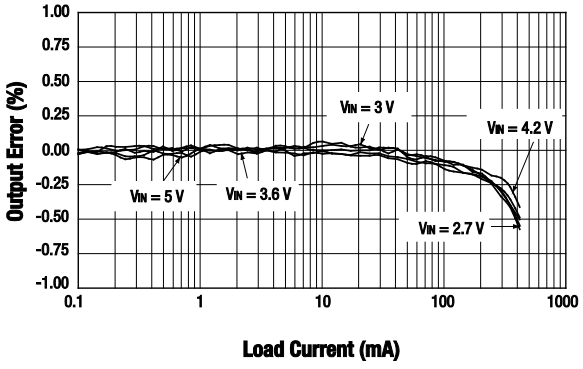


Figure 6. Load Regulation (V_{OUT} = 1.8 V, L = 2.2 µH)

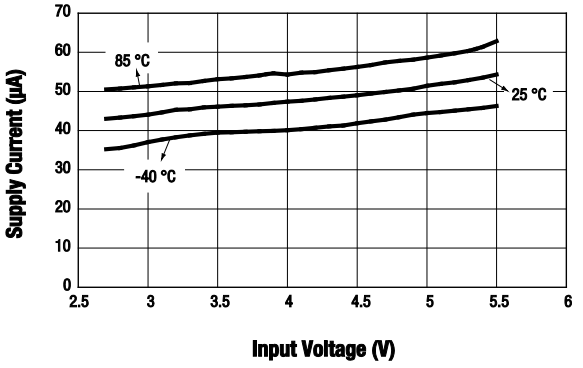


Figure 7. No Load Quiescent Current vs Input Voltage

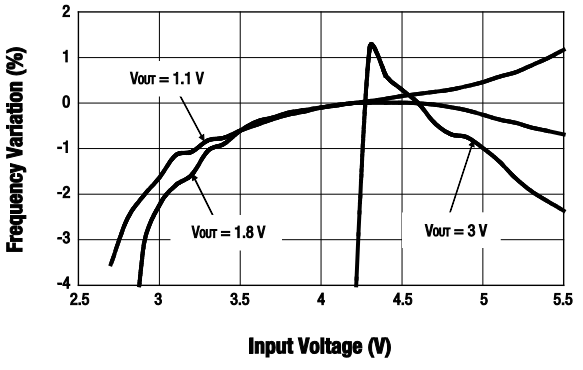


Figure 8. Switching Frequency vs Input Voltage

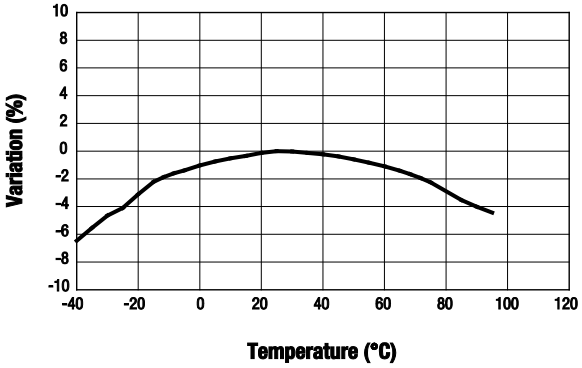


Figure 9. Switching Frequency Variation vs Temperature

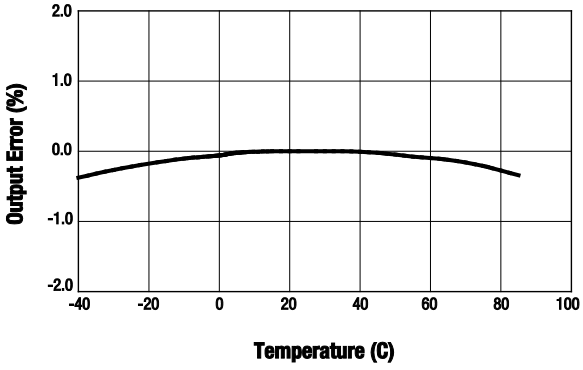


Figure 10. Output Voltage Error vs Temperature (V_{IN} = 3.6 V, V_{OUT} = 1.8 V, I_{OUT} = 400 mA)

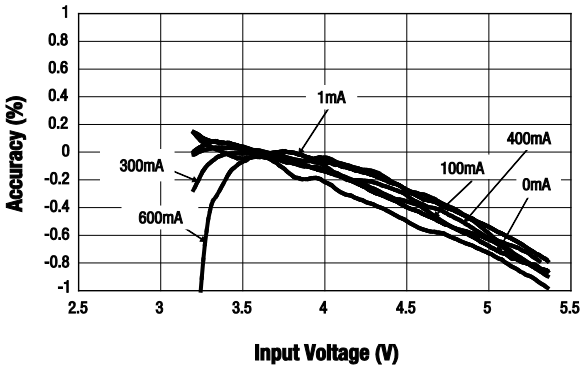


Figure 11. Line Regulation (V_{OUT} = 3 V)

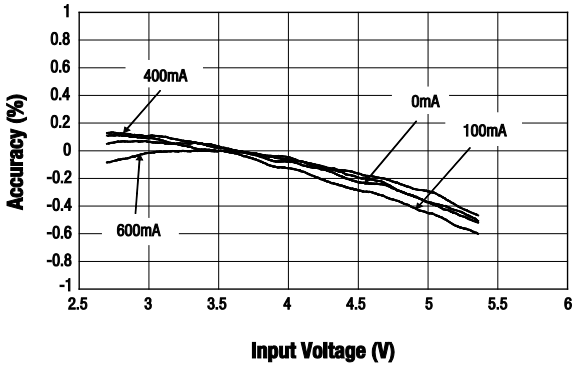


Figure 12. Line Regulation (V_{OUT} = 1.8 V)

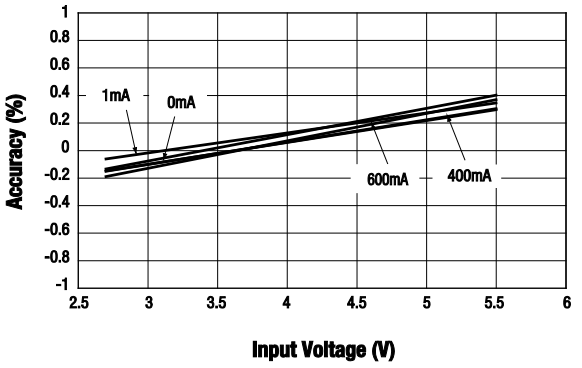


Figure 13. Line Regulation (V_{OUT} = 1.1 V)

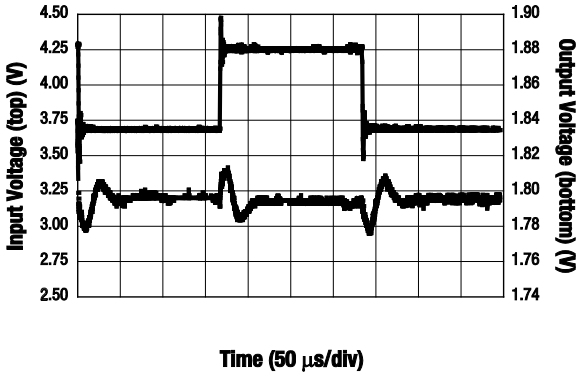


Figure 14. Line Transient (V_{OUT} = 1.8 V; 400 mA Load; No Feed Forward Capacitor)

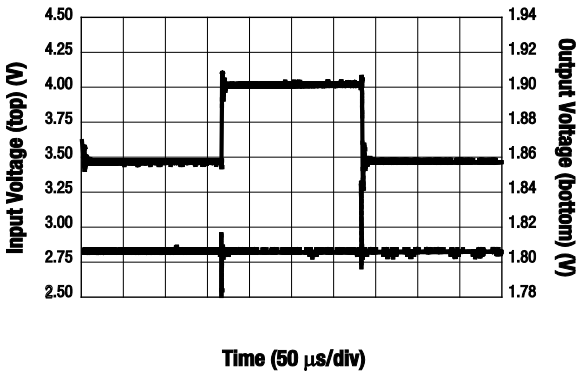


Figure 15. Line Transient
(VOUT = 1.8 V; No Feed Forward Capacitor)

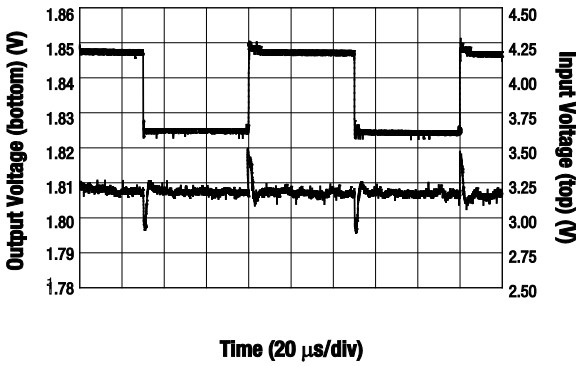


Figure 16. Line Transient (VOUT = 1.8 V; CFF = 100 pF)

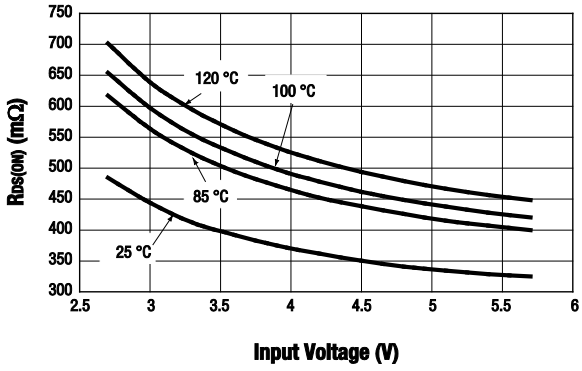


Figure 17. N-Channel RDS(ON) vs Input Voltage

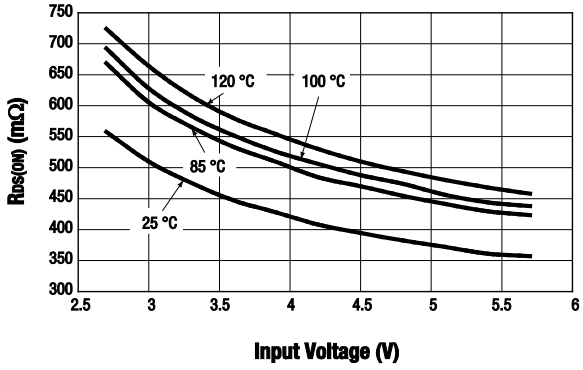


Figure 18. P-Channel RDS(ON) vs Input Voltage

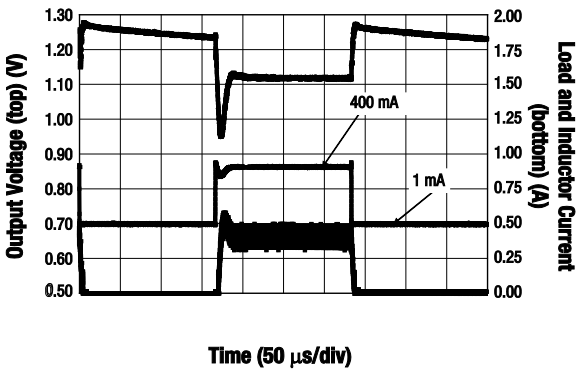


Figure 19. Load Transient
(VOUT = 1.1 V; No Feed Forward Capacitor)

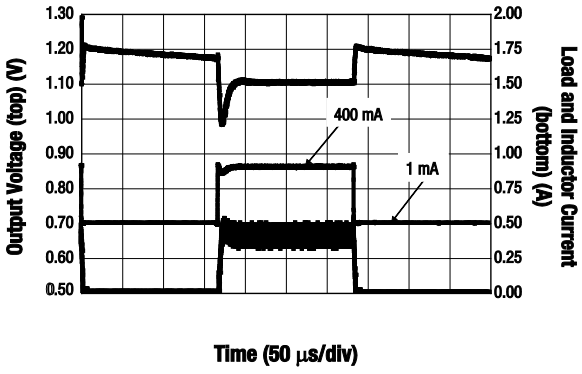


Figure 20. Load Transient (Vout = 1.1 V; CFF = 100 pF)

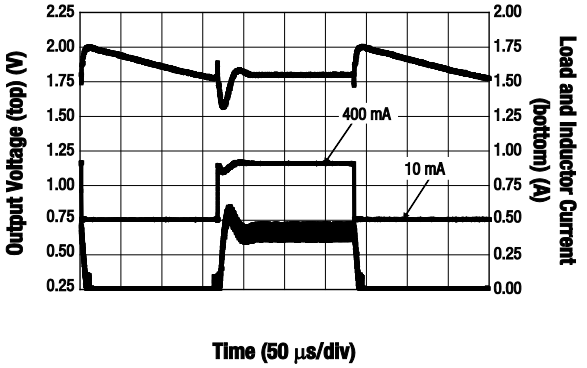


Figure 21. Load Transient
(V_{OUT} = 1.8 V; No Feed Forward Capacitor)

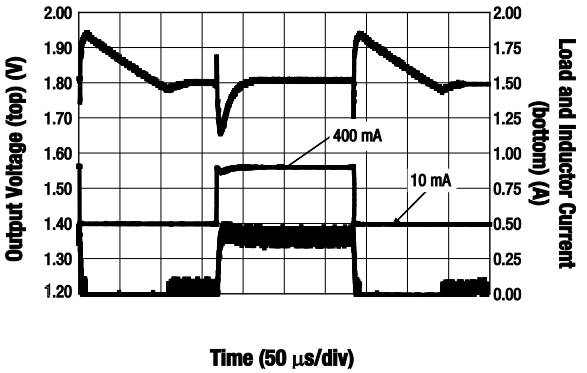


Figure 22. Load Transient (V_{OUT} = 1.8 V; C_{FF} = 100 pF)

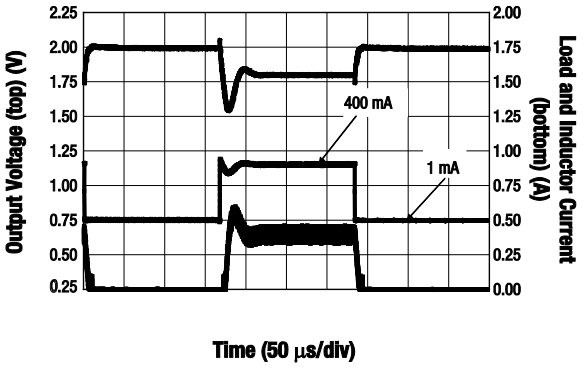


Figure 23. Load Transient
(V_{OUT} = 1.8 V; No Feed Forward Capacitor)

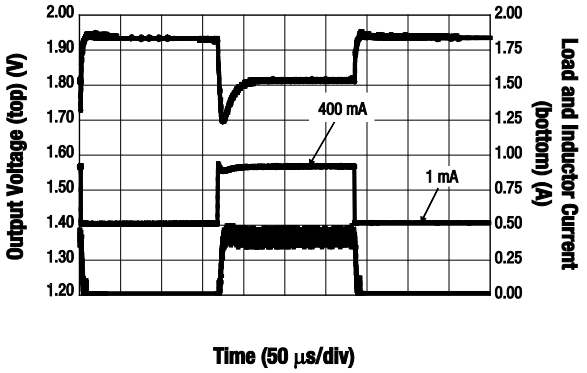


Figure 24. Load Transient (V_{OUT} = 1.8 V; C_{FF} = 100 pF)

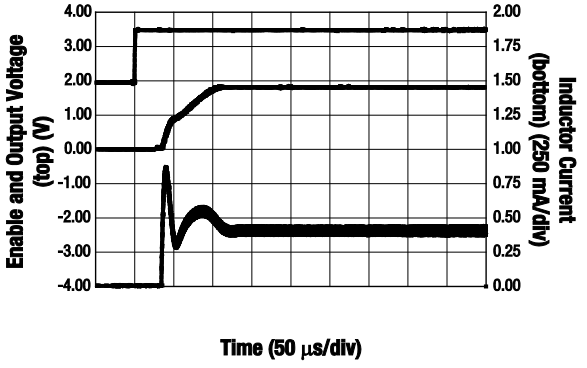


Figure 25. Soft Start
(V_{OUT} = 1.8 V; No Feed Forward Capacitor)

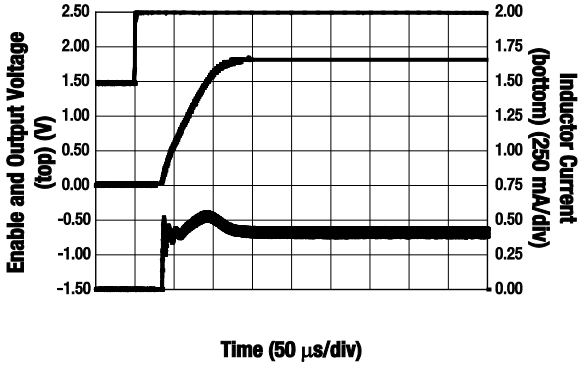


Figure 26. Soft Start
(V_{OUT} = 1.8 V; C_{FF} = 100 pF)

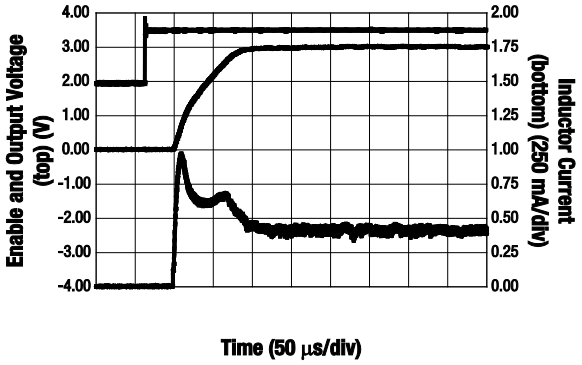


Figure 27. Soft Start
(V_{OUT} = 3 V; No Feed-Forward Capacitor)

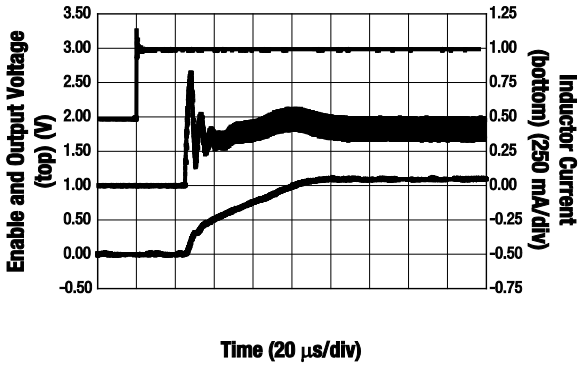


Figure 28. Load Transient
(V_{OUT} = 1.1 V; No Feed-Forward Capacitor)

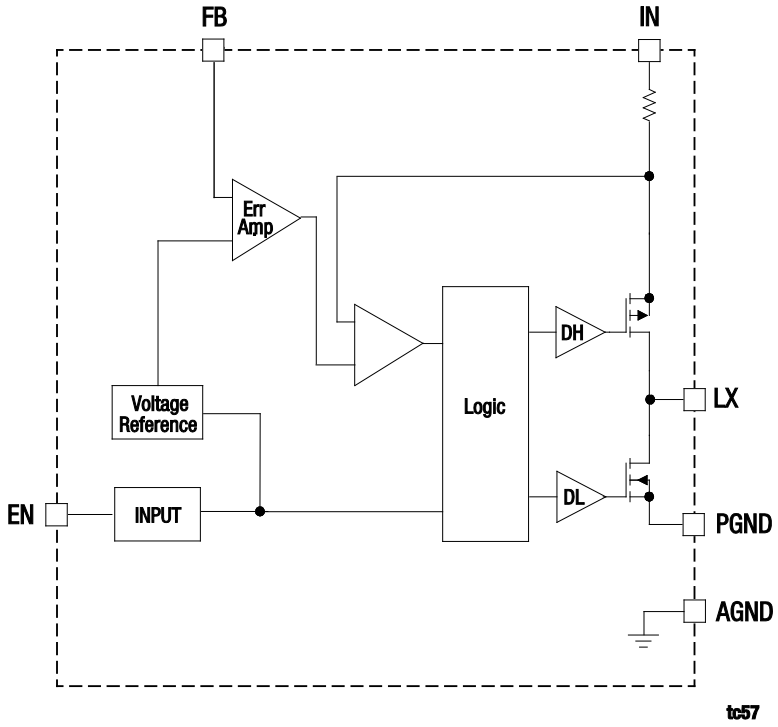


Figure 29. AAT1149 Functional Block Diagram

Functional Description

The AAT1149 is a high performance 400 mA, 3.0 MHz monolithic step-down converter. It minimizes external component size, enabling the use of a tiny 0603 inductor that is only 1 mm tall, and optimizes efficiency over the complete load range. Apart from the small bypass input capacitor, only a small L-C filter is required at the output. Typically, a 1.8 µH inductor and a 4.7 µF ceramic capacitor are recommended (see Tables of values). A functional block diagram is provided in Figure 29.

Only three external power components (C_{IN}, C_{OUT}, and L) are required. Output voltage is programmed with external feedback resistors, ranging from 1.0 V to the input voltage. An additional feed-forward capacitor can also be added to the external feedback to provide improved transient response (see Figure 31).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high-side MOSFET.

The input voltage range is 2.7 V to 5.5 V. The converter efficiency has been optimized for all load conditions, ranging from no load to 400 mA.

The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Control Loop

The AAT1149 is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection. A fixed slope compensation signal is added to the sensed current to maintain stability for duty cycles greater than 50%. The peak current mode loop appears as a voltage-programmed current source in parallel with the output capacitor.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the transconductance voltage error amplifier output. For the adjustable output, the error amplifier reference is fixed at 0.6 V.

Soft Start/Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When the EN pin is pulled low, it forces the AAT1149 into a low-power, non-switching state. The total input current during shutdown is less than 1 μA.

Current Limit and Over-Temperature Protection

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

Thermal protection completely disables switching when internal dissipation becomes excessive. The junction over-temperature threshold is 140 °C with 15 °C of hysteresis. Once an over-temperature or over-current fault condition is removed, the output voltage automatically recovers.

Under-Voltage Lockout

Internal bias of all circuits is controlled using the IN input. Under-Voltage Lockout (UVLO) guarantees sufficient V_{IN} bias and proper operation of all internal circuitry before activation.

Applications Information

Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements. Table 4 displays suggested inductor values for various output voltages.

Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high Direct Current Resistance (DCR). Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

The 1.8 μH CDRH2D09 series inductor from Sumida has a 131 mΩ DCR and a 400 mA saturation current rating. At full load, the inductor DC loss is 21 mW which gives a 2.8% loss in efficiency for a 400 mA, 1.8 V output.

Table 4. AAT1149 Suggested Inductor Values For Various Output Voltages

Output Voltage (V)	Typical Inductor Value (μH)
1.0 and 1.2	1.0 to 1.2
1.5 and 1.8	1.5 to 1.8
2.5	2.2 to 2.7
3.3	3.3

Input Capacitor

Select a 4.7 µF to 10 µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (VPP) and solve for C. The calculated value varies with input voltage and is a maximum when VIN is double the output voltage.

$$C_{IN} = \frac{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_S}$$

$$\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1}{4} \quad \text{for} \quad V_{IN} = 2 \times V_{OUT}$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times 4 \times f_S}$$

Where *fs* is the switching frequency. Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10 µF, 6.3 V, X5R ceramic capacitor with 5.0 VDC applied is actually about 6 µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and always is less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} = \sqrt{D \times (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

for VIN = 2 × VOUT

$$I_{RMS(MAX)} = \frac{I_{OUT}}{2}$$

The term $\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when VOUT is twice VIN. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT1149. Low Equivalent Series Resistance/Equivalent Series Inductance (ESR/ESL) X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the AAT1149. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple.

The proper placement of the input capacitor (C2) can be seen in the Evaluation Board layout in Figure 32.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the Evaluation Board input voltage pins. The inductance of these wires, along with the low ESR ceramic input capacitor, can create a high-Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result.

Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR, ESL bypass ceramic. This dampens the high-Q network and stabilizes the system.

Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 4.7 µF to 10 µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient (ΔILOAD) is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

The internal voltage loop compensation also limits the minimum output capacitor value to 4.7 µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance reduces the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS\,(MAX)} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{L \times f_S \times V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

Feedback Resistor Selection

Resistors R1 and R2 in Figure 31 program the output to regulate at a voltage higher than 0.6 V. To limit the bias current required for the external feedback resistor string while maintaining good noise immunity, the minimum suggested value for R2 is 59 kΩ. Although a larger value can further reduce quiescent current, it also increases the impedance of the feedback node, making it more sensitive to external noise and interference.

Table 5 summarizes the resistor values for various output voltages with R2 set to either 59 kΩ for good noise immunity or 121 kΩ for reduced no-load input current.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R2 = \left(\frac{1.5V}{0.6V} - 1\right) \times 59k\Omega = 88.5k\Omega$$

The AAT1149, combined with an external feed-forward capacitor (C3 in Figure 31), delivers enhanced transient response for extreme pulsed load applications. The addition of the feed-forward capacitor typically requires a larger output capacitor C1 for stability.

Table 5. Feedback Resistor Values

V_{OUT} (V)	R1 (kΩ) (R2 = 59 kΩ)	R1 (kΩ) (R2 = 121 kΩ)
1.00	39.2	80.6
1.10	49.9	100
1.20	59.0	121
1.30	68.1	140
1.40	78.7	162
1.50	88.7	182
1.80	118	243
1.85	124	255
2.00	137	280
2.50	187	383
3.30	267	549

Thermal Calculations

There are three types of losses associated with the AAT1149 step-down converter: conduction losses, switching losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming Continuous Conduction Mode (CCM), a simplified form of the losses is given by:

$$P_{TOTAL} = \frac{I_{OUT}^2 \times \left(R_{DS(ON)H} \times V_{OUT} + R_{DS(ON)L} \times \left[V_{IN} - V_{OUT}\right]\right)}{V_{IN}} + \left(t_{SW} \times f_S \times I_{OUT} + I_Q\right) \times V_{IN}$$

I_Q is the step-down converter quiescent current. The term t_{SW} is used to estimate the full load step-down converter switching losses.

For the condition where the step-down converter is in dropout at 100% duty cycle, the total device dissipation reduces to:

$$P_{TOTAL} = I_{OUT}^2 \times R_{DS(ON)H} + I_Q \times V_{IN}$$

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the SC70JW-8 package, which is 160 °C/W.

$$T_{J(MAX)} = P_{TOTAL} \times \theta_{JA} + T_A$$

Layout

The suggested PCB layout for the AAT1149 is shown in Figure 32. The following guidelines should be used to help ensure a proper layout.

1. The input capacitor (C2) should connect as closely as possible to IN (pin 3) and PGND (pins 6, 7, and 8).
2. C1 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or FB pin (pin 2) should be separate from any power trace and connect as closely as possible to the load point. Sensing along a high-current load trace degrades DC load regulation. If external feedback resistors are used, they should be placed as closely as possible to the FB pin (pin 2) to minimize the length of the high impedance feedback trace.
4. The resistance of the trace from the load return to PGND (pins 6, 7, and 8) should be kept to a minimum. This helps to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. A pad thickness of less than 1 mm is recommended to achieve higher stand-off. A high density, small footprint layout can be achieved using an inexpensive, miniature, non-shielded, high DCR inductor, as shown in Figure 30.

Evaluation Board Description

The AAT1149 Evaluation Board schematic diagram is provided in Figure 31. The PCB layer details are shown in Figure 32.

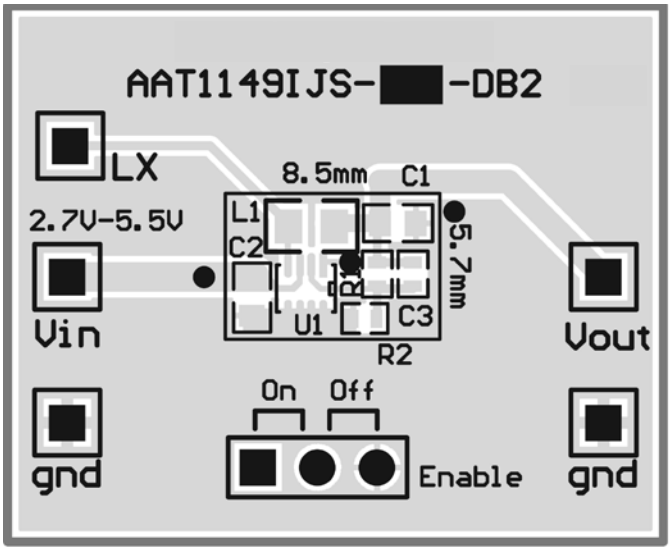


Figure 30. Minimum Evaluation Board Footprint
Using 2.0 × 1.25 × 1.0 mm Inductor

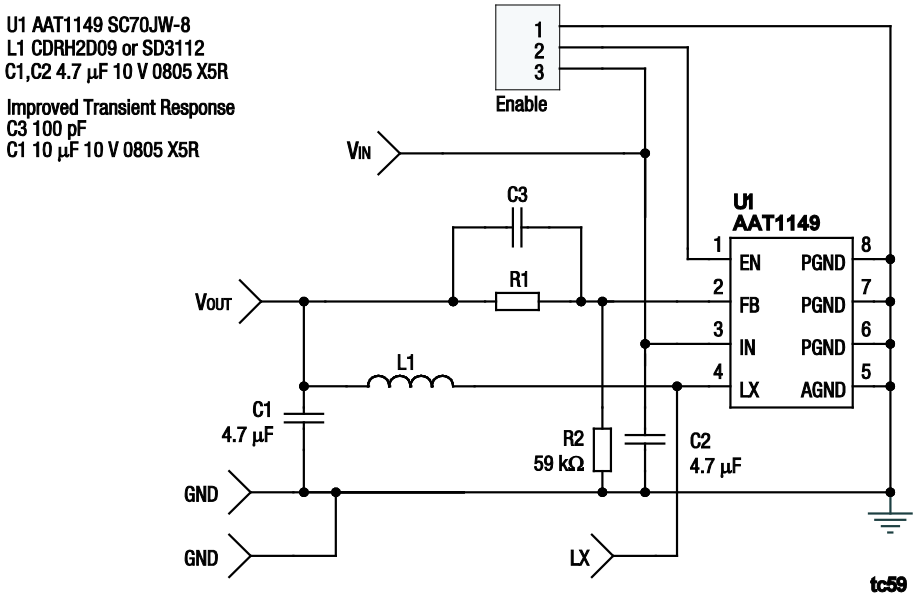
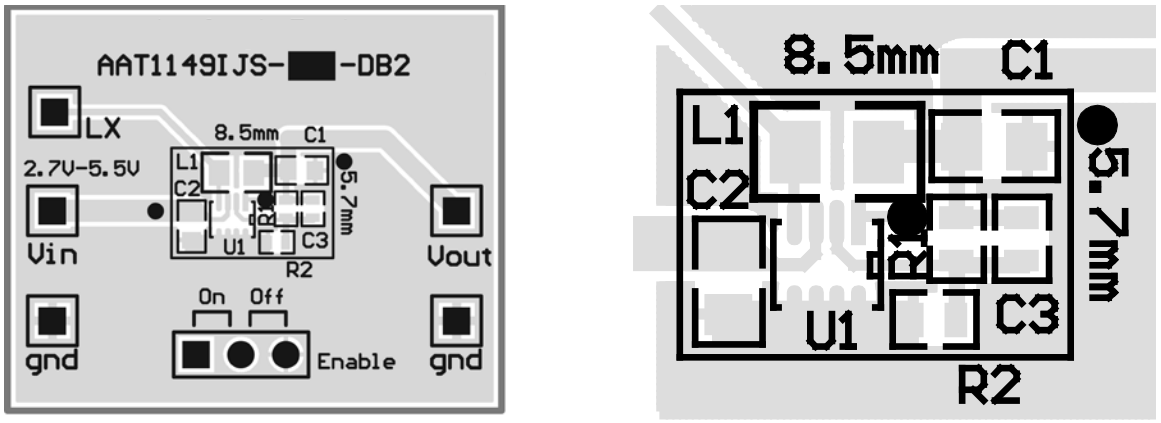


Figure 31. AAT1149 Evaluation Board Schematic



Top Side

Exploded View of Top Side

Bottom Side

tc60

Figure 32. AAT1149 Evaluation Board Layer Details

Step-Down Converter Design Example

Specifications

V_{OUT} = 1.8 V @ 400 mA, pulsed load ΔI_{LOAD} = 300 mA

V_{IN} = 2.7 V to 4.2 V (3.6 V nominal)

f_S = 3.0 MHz

T_A = 85 °C

1.8 V Output Inductor

$$L1 = 1\frac{\mu s}{A} \times V_{OUT} = 1\frac{\mu s}{A} \times 1.8V = 1.8\mu H$$

For Taiyo Yuden inductor CBC2518T2R2M, 2.2 µH, DCR = 130 mΩ.

$$\Delta I_{L1} = \frac{V_{OUT}}{L1 \times f_S} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) = \frac{1.8V}{2.2\mu H \times 3.0MHz} \times \left(1 - \frac{1.8V}{4.2V}\right) = 156mA$$

$$I_{PKL1} = I_{OUT} + \frac{\Delta I_{L1}}{2} = 0.4V + 0.078A = 0.478A$$

Where, I_{PKL1} is the peak current on L1.

$$P_{L1} = I_{OUT}^2 \times DCR = 0.4A^2 \times 130m\Omega = 21mW$$

1.8V Output Capacitor

V_{DROOP} = 0.1 V

$$C_{OUT} == \frac{3 \times \Delta I_{LOAD}}{V_{DROOP} \times f_S} = \frac{3 \times 0.3A}{0.1V \times 3.0MHz} = 3.0\mu H,\ \ use\ 4.7\mu F$$

$$I_{RMS} = \frac{1}{2\sqrt{3}} \times \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{L1 \times f_S \times V_{IN(MAX)}} = \frac{1}{2\sqrt{3}} \times \frac{1.8V \times \left(4.2V - 1.8V\right)}{2.2\mu H \times 3.0MHz \times 4.2V} = 45mArms$$

$$P_{ESR} = ESR \times I_{RMS}^2 = 5m\Omega \times (45mA)^2 = 10\mu W$$

Input Capacitor

Input Ripple V_{PP} = 25 mV

$$C_{IN} = \frac{1}{4 \times \left(\frac{V_{PP}}{I_{OUT}} - ESR\right) \times f_S} = \frac{1}{4 \times \left(\frac{25mV}{0.4A} - 5m\Omega\right) \times 3.0MHz} = 1.45\mu F\ ,\ use\ 2.2\mu F$$

$$I_{RMS} = \frac{I_{OUT}}{2} = 0.2Arms$$

$$P = ESR \times I_{RMS}^2 = 5m\Omega \times (0.2A)^2 = 0.2mW$$

AAT1149 Losses

$$P_{TOTAL} = \frac{I_{OUT}^2 \times \left(R_{DS(ON)H} \times V_{OUT} + R_{DS(ON)L} \times \left[V_{IN} - V_{OUT}\right]\right)}{V_{IN}} + \left(t_{SW} \times f_S \times I_{OUT} + I_Q\right) \times V_{IN}$$

$$= \frac{0.4^2 \times \left(0.725\Omega \times 1.8V + 0.7\Omega \times \left[4.2V - 1.8V\right]\right)}{4.2V} + \left(5ns \times 3MHz \times 0.4A + 70\mu A\right) \times 4.2V = 140mW$$

$$T_{J(MAX)} = P_{LOSS} \times \theta_{JA} + T_A = \left(160°C/W\right) \times 140mW + 85°C = 107°C$$

Table 6 summarizes the feedback resistor values for various output voltages. Tables 7 and 8 list the typical surface mount inductors and surface mount capacitors.

Table 6. Feedback Resistor Values

V_{OUT} (V)	R1 (kΩ) (R2 = 59 kΩ)	R1 (kΩ) (R2 = 121 kΩ)☐	L1 (µH)
1.0	39.2	80.6	1.0
1.2	59.0	121	1.2
1.5	88.7	182	1.5
1.8	118	243	1.8
2.5	187	383	2.2
3.3	267	549	3.3

Table 7. Typical Surface Mount Inductors

Manufacturer	Part Number/Type	Inductance (µH)	Rated Current (mA)	DCR (Ω)	Size (mm) L×W×H
Taiyo Yuden	BRC1608	1.0	520	180	0603 (height = 1 mm)
		1.5	410	300	
	BRL2012	1.5	600	200	0805 (height = 1 mm)
		2.2	550	250	
		3.3	450	350	
	CBC2518 Wire wound chip	1.0	1000	80	2.5×1.8×1.8
		2.2	890	130	
Sumida	CDRH2D09 Shielded	1.2	590	97.5	3.2×3.2×1.0
		1.5	520	110	
		1.8	480	131	
		2.5	440	150	
		3.0	400	195	
Murata	LQH2MCN4R7M02 Unshielded	1.0	485	300	2.0×1.6×0.95
		1.5	445	400	
		2.2	425	480	
		3.3	375	600	
Coiltronics	SD3118 Shielded	1.2	720	75	3.15×3.15×1.2
		1.5	630	104	
		2.2	510	116	
		3.3	430	139	

Table 8. Typical Surface Mount Capacitors

Manufacturer	Part Number	Value (µF)	Voltage (V)	Temperature Coefficient	Case
Murata	GRM219R61A475KE19	4.7	10	X5R	0805
Murata	GRM21BR60J106KE19	10	6.3	X5R	0805
Murata	GRM185R60J475M	4.7	6.3	X5R	0603

Package Information

Package dimensions and shown in Figure 33, and tape and reel dimensions are provided in Figure 34.

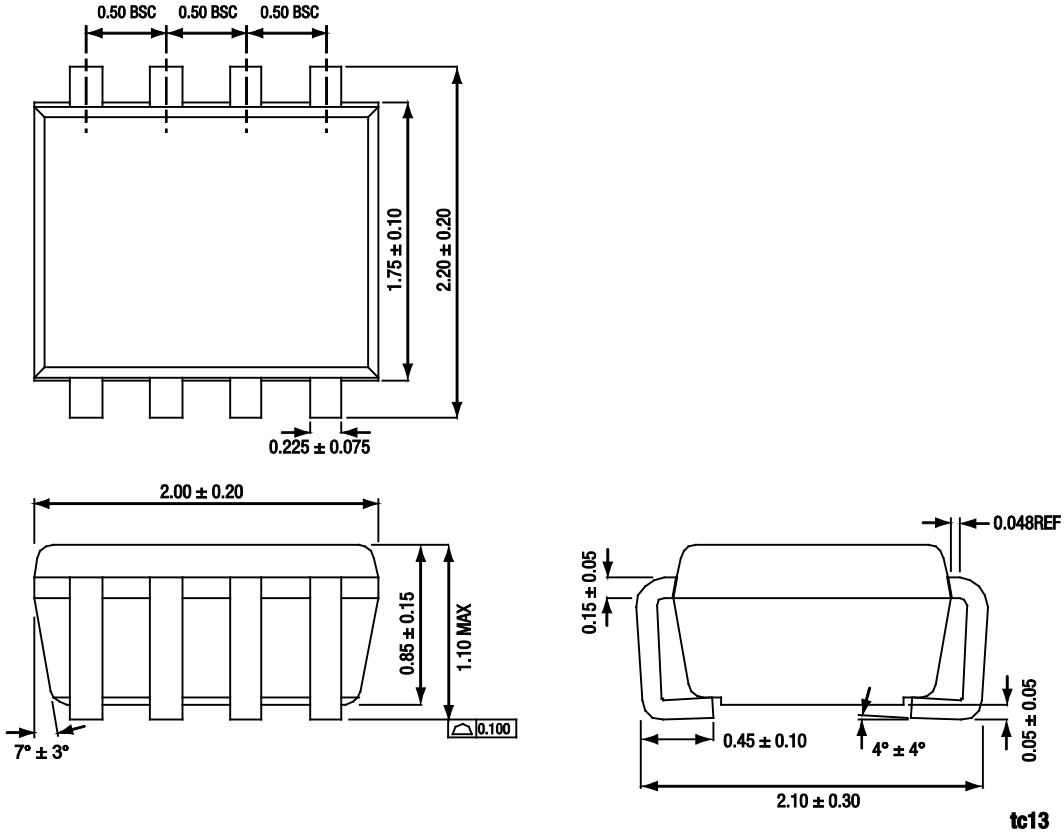


Figure 33. AAT1149 8-pin SC70JW Package Dimensions

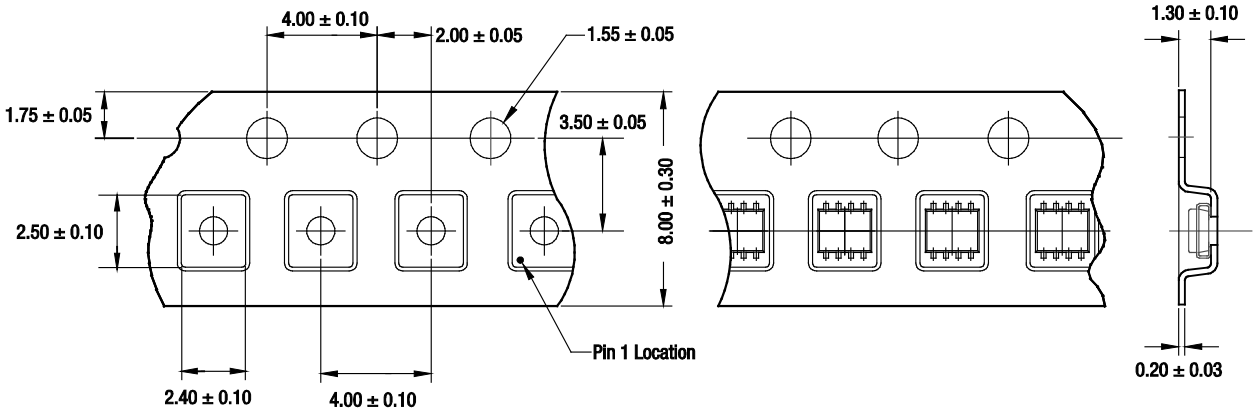


Figure 34. AAT1149 Carrier Tape Dimensions

Ordering Information

Model Name	Manufacturing Part Number (Note 1)	Evaluation Board Part Number
AAT1149 Fast Transient Step-Down Converter	**AAT1149IJS-0.6-T1**	AAT1149IJS-0.6-EVB

Note 1: Sample stock is generally held on the part number listed in **BOLD**.